2814

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QUERY CONTROL FORM				RTIS USE ONLY	
Application No.	10/084,810	Prepared by	N.H.	Tracking Number	05882143
Examiner-GAU	Fahmy - 2814	Date	1-30-4	Week Date	12/29/03
		No. of queries	2	IFW	

JACKET			
a. Serial No.	f. Foreign Priority	k. Print Claim(s)	(p. PTO-1449)
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	(o. PTO-892)	t. Other

SPECIFICATION

a. Page Missing
b. Text Continuity
c. Holes through Data
d. Other Missing Text
e. Illegible Text
f. Duplicate Text
g. Brief Description
h. Sequence Listing
i. Appendix
j. Amendments
k. Other

CLAIMS

a. Claim(s) Missing
b. Improper Dependency
c. Duplicate Numbers
d. Incorrect Numbering
e. Index Disagrees
f. Punctuation
g. Amendments
h. Bracketing
i. Missing Text
j. Duplicate Text
(k. Other) Illegible

MESSAGE

① Please provide at least one PTO-892 and/or PTO-1449's in file.

② Claims from PTO are illegible, Please provide.

- Legible claims are in the IFW file.

Thankyou

initials N.H.

RESPONSE

- PTO-892 (2 pages).
- Legible claims are included.

Dilu Nguyen
4/6/04

initials

E-5 (Rev. 10/01/02)

Notice of References Cited	Application/Control No. 10/084,810	Applicant(s)/Patent Under Reexamination LIU ET AL.	
	Examiner DiLinh Nguyen	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6025640	02-2000	Yagi et al.	257
	B	US-5807610	09-1998	Cox et al.	427
	C	US-6380062	04-2003	Liu	438
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
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	S					
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NON-PATENT DOCUMENTS

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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	Examiner DiLinh Nguyen	Art Unit 2814	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5656550	08-1997	Tsuji et al.	438
	B	US-5807610	09-1998	Cox et al.	427
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
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In the Claims:

15. (currently amended) A method for forming an integrated circuit package that contains an array of metal pegs connected by printed circuit lines, comprising the steps of:

providing a metal substrate that has a first surface and a second surface;

forming a plurality of first electroplate layers on the first surface and forming a plurality of second electroplate layers on the second surface;

forming a mask layer over the first surface to form a die pad region so that the first electroplate layers are positioned around the die pad region;

etching the exposed metal substrate on the first surface using the mask layer and the first electroplate layers as an etching mask to form a die pad and a plurality of first metal pegs;

removing the mask layer;

attaching a silicon die ~~over~~ onto the die pad, and connecting the die and the first electroplate layers electrically, wherein an area of the die pad region is smaller than ~~the~~ an area of the die;

enclosing the die, the die pad, the first electroplate layers and the first metal pegs above the first surface of the metal substrate with an insulating material;

forming a plurality of circuit line masks on the second surface of the metal substrate; and

etching the exposed metal substrate on the second surface using the second electroplate layers and the circuit line mask as an etching mask to ~~from~~ form a plurality of second metal pegs and a plurality of printed circuit lines.

16. (original) The method of claim 15, wherein the step of forming the first electroplate layers and the second electroplate layers further includes:

forming a first photoresist layer and a second photoresist layer over the first surface and the second surface of the metal substrate, respectively;

carrying out exposure and development operations with regards to the first and the second photoresist layers, respectively, so that a portion of the first surface and a portion of the second surface are exposed, thus defining a plurality of first metal pegs regions and a plurality of second metal pegs regions; and

conducting an electroplating operation to form first electroplate layers and second electroplate layers over the first metal peg regions and the second metal peg regions, respectively.

17. (original) The method of claim 16, wherein after the step of forming the first electroplate layers and the second electroplate layers, but before the step of forming the mask layer, further includes removing the first photoresist layer.

18. (original) The method of claim 15, wherein the step of forming the first electroplate layers includes electroplating a material chosen from a group consisting of gold, silver, nickel, palladium and a combination of them.

19. (original) The method of claim 15, wherein the step of forming the second electroplate layer includes electroplating gold, silver, nickel, palladium or a combination of them.

20. (original) The method of claim 15, wherein the step of forming the mask layer includes:

forming a photoresist layer over the first surface of the metal substrate; and

exposing the photoresist layer and developing the photoresist layer to form the mask layer.

21. (original) The method of claim 15, wherein the step of forming the circuit line masks includes using a screen printing method.

22. (original) The method of claim 15, wherein after the step of forming the printed circuit lines, further includes forming a plurality of sidewall masks on the sidewalls of the circuit lines.

23. (original) The method of claim 22, wherein the step of forming the sidewall masks includes using a screen printing method.

24. (original) The method of claim 15, wherein after the step of forming the printed circuit lines, further includes attaching a solder ball to the surface of each second electroplate layer.

25. (original) The method of claim 15, wherein after the step of forming the printed circuit lines, further includes attaching a copper ball to the surface of each second electroplate layer.

26. (original) The method of claim 15, wherein after the step of forming the printed circuit lines, further includes smearing solder paste over the surface of each second electroplate layer.

27. (currently added) The method of claim 15, wherein the die, the die pad, the first electroplate layers and the first metal pegs above the first surface of the metal substrate are enclosed in one molding operation.